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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	6

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,331	JARVIS, ANTHONY X.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9, and 19-24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Chen et al., US Patent 4,851,993, cited as a prior art reference in paper number 5, item number AA, filed on August 5, 2002.

4. Referring to claim 1, Chen et al. have taught a data processor comprising:

a. an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline (Column 9, lines 17-27);

b. a data cache capable of storing data values used by said pending instruction (Figure 1, element 121);

c. a plurality of architectural registers capable of receiving said data values from said data cache (Abstract, There are inherently a plurality of architectural registers that

the executing instructions access that are capable of receiving data values, or operand values from said data cache. See Hennessey, pages 70-73 and pages 191-194);

d. bypass circuitry capable of transferring a first data value from said data cache directly to a functional unit in one of said N processing stages without first storing said first data value in a destination one of said plurality of architectural registers (Abstract, column 3 lines 1-8); and

e. a cache refill controller capable of detecting that a cache miss has occurred at a first address associated with said first data value (Abstract, column 3 lines 1-8), receiving a missed cache line from a main memory coupled to said data processor, and causing said first data value to be transferred from said missed cache line to said functional unit (Abstract, column 3 lines 1-8).

5. Referring to claim 2, Chen et al. have taught the data processor as set forth in claim 1, as described above, and wherein said cache refill controller is further capable of stalling said instruction execution pipeline after said cache miss by halting clock signals driving said instruction execution pipeline (Column 6, lines 41-57).

6. Referring to claim 3, Chen et al. have taught the data processor as set forth in claim 2, as described above, and further comprising a clock controller coupled to said cache refill controller and capable of generating said clock signals driving said instruction execution pipeline, wherein said clock controller stalls said instruction execution pipeline by halting said clock signals in response to a command from said cache refill controller (Column 6, lines 41-57).

7. Referring to claim 4, Chen et al. have taught the data processor as set forth in claim 3, as described above, and wherein said cache refill controller causes said first data value to be

transferred to said functional unit when said instruction execution pipeline is stalled (Abstract, column 3 lines 1-8, column 6, lines 41-57).

8. Referring to claim 5, Chen et al. have taught the data processor as set forth in claim 4, as described above, and wherein said cache refill controller is further capable of storing said missed cache line into said data cache (Column 4, lines 37-66).

9. Referring to claim 6, Chen et al. have taught the data processor as set forth in claim 5, as described above, and wherein said cache refill controller causes said first data value to be transferred to said functional unit by retrieving said first data value from said missed cache line stored in said data cache (Column 6, lines 41-57).

10. Referring to claim 7, Chen et al, have taught the data processor as set forth in claim 6, as described above, and wherein said cache refill controller causes said first data value to be transferred to said functional unit after said cache miss via said bypass circuitry (Abstract, column 3 lines 1-8).

11. Referring to claim 8, Chen et al. have taught the data processor as set forth in claim 7, as described above, wherein said clock controller generates an early clock signal when said execution pipeline is stalled, wherein said early clock signal causes said first data value to be transferred to said functional unit from said data cache (Column 7, line 60-column 8, line10).

12. Referring to claim 9, Chen et al. have taught the data processor as set forth in claim 8 wherein said cache refill controller restarts said instruction execution pipeline after said clock controller generates said early clock signal (Column 7, line 60-column 8, line10, Abstract, column 3 lines 1-8, column 6, lines 41-57).

13. Claim 19 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

14. Claim 20 does not recite limitations above the claimed invention set forth in claim 2 and is therefore rejected for the same reasons set forth in the rejection of claim 2 above.

15. Claim 21 does not recite limitations above the claimed invention set forth in claim 5 and is therefore rejected for the same reasons set forth in the rejection of claim 5 above.

16. Claim 22 does not recite limitations above the claimed invention set forth in claim 6 and is therefore rejected for the same reasons set forth in the rejection of claim 6 above.

17. Claim 23 does not recite limitations above the claimed invention set forth in claim 7 and is therefore rejected for the same reasons set forth in the rejection of claim 7 above.

18. Referring to claim 24, Chen et al have taught the method as set forth in claim 23, as described above, and further comprising the step of restarting the instruction execution pipeline after completion of the sub-step of transferring the first data value to the functional unit after the cache miss via the bypass circuitry (Column 7, line 60-column 8, line10, Abstract, column 3 lines 1-8, column 6, lines 41-57).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al., US Patent 4,851,993, cited as a prior art reference in paper number 5, item number AA, filed on August 5, 2002., in view of Boettner et al., US Patent 4,777,589.

21. Referring to claim 10, Chen et al. have taught a processing system comprising:

a. a data processor (Abstract, Figure 1);

b. a memory coupled to said data processor (Figure 1, element 103);

c. wherein said data processor comprises:

i. an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline (Column 9, lines 17-27);

ii. a data cache capable of storing data values used by said pending instruction (Figure 1, element 121);

iii. a plurality of architectural registers capable of receiving said data values from said data cache (Abstract, There are inherently a plurality of architectural registers that the executing instructions access that are capable of receiving data values, or operand values from said data cache. See Hennessey, pages 70-73 and pages 191-194);

iv. bypass circuitry capable of transferring a first data value from said data cache directly to a functional unit in one of said N processing stages without first storing said first data value in a destination one of said plurality of architectural registers (Abstract, column 3 lines 1-8); and

v. a cache refill controller capable of detecting that a cache miss has occurred at a first address associated with said first data value, receiving a missed cache line from a main memory coupled to said data processor, and causing said first data value to be transferred from said missed cache line to said functional unit (Abstract, column 3 lines 1-8).

22. Chen et al. have not specifically taught a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor. However, Boettner et al. have taught a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor (Boettner et al., column 1, lines 22-39) in order to access I/O devices by procedures implemented in a higher level language. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Chen et al. include a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor, as taught by Boettner et al. for the desirable purpose of accessing I/O devices by procedures implemented in a higher level language (Boettner et al., column 1, lines 22-39).

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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